REMARKS

Claims 1-10 and 12-53 are pending. Claims 1, 12, and 24 have been amended. Claim 54 has been added.

Claims 1-5, 8-10, 12-18, and 31-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,624,850) ("Guidash") in view of Dierickx (U.S. Patent No. 7,106,373) ("Dierickx"). The rejection is respectfully traversed.

Claim 1 recites a method of operating a pixel circuit. The method comprises, "accumulating photo-generated charge during an integration period; partially turning on a transfer transistor to remove some of said accumulated photo-generated charge to a floating diffusion node, wherein the transfer transistor is coupled between an element configured to generate electrical charge in response to incident light and a column output line; turning on a reset transistor during the integration period to remove said some of said accumulated photo-generated charge from said floating diffusion node; turning on the reset transistor just before the end of the integration period to reset said floating diffusion node; fully turning on the transfer transistor at the end of the integration period to remove all of said accumulated photo-generated charge to the floating diffusion node; and producing an output signal based at least in part on a charge in the floating diffusion region at the end of said integration period."

The Office Action relies upon Guidash as disclosing certain structural elements of the claimed invention, but the Office Action correctly concludes, "Guidash does not disclose a method for operating the pixel circuit as claimed." (Page 3) Therefore, the Office Action relies on Guidash in combination with Dierickx.

Dierickx discloses a pixel circuit in which charge is removed from a charge storage node 37 associated with a photodiode 32 to a reset voltage line via a reset transistor 31 modulated by a "reference" voltage applied to a "reference" transistor between the photodiode and the reset transistor. (Dierickx, FIG. 3 and Column 6, Lines 51-64)

Contrary to the Office Action's assertion, Dierickx does not teach "that a reference voltage should be applied to *a* transistor between the reset transistor and the photodiode...." (Page 4) Dierickx teaches that an *additional* "reference" transistor must be added to the pixel circuit to modulate a reset transistor. (See, e.g., FIG. 3) Thus, it would not have been obvious to combine Pain in Dierickx in the manner claimed. Rather, the obvious way to combine the references would be to add a "reference" transistor to the Guidash pixel circuit between the reset transistor and the photogate or photodiode, just as illustrated in Dierickx's FIG. 3. Applicants' claimed invention improves upon this design by eliminating the need for this additional "reference" transistor. Among other things, this reduces fabrication costs. Dierickx does not teach or suggest turning on an existing transistor (e.g., the transfer transistor) "to remove some of said accumulated photo-generated charge to a floating diffusion node" and, thus, fails to achieve the efficiency of Applicants' design.

Moreover, if the voltages taught by Dierickx were applied a transfer transistor of a 4T or 5T pixel circuit, the pixel circuit would cease to operate correctly and produce pixel values with excessive noise. In 4T and 5T pixel designs a transfer transistor (e.g., element 103 of Applicants' FIG. 2A) is used to selectively transfer charge accumulated at a photodiode (e.g., element 113 of Applicants' FIG. 2A) to a floating diffusion node (e.g., element 112 of Applicants' FIG. 2A). The charge is subsequently read-out from the floating diffusion node via the column output line (e.g., element 160 of Applicants' FIG. 2A) and combined with other pixel signal values to form an image.

To reduce noise in the resulting image, the floating diffusion node must be reset before charge to be readout is transferred from the photodiode. This is accomplished by pulsing the reset transistor just before the end of the integration period. See, for example, the fourth pulse applied to the reset transistor (RST) in Applicants' FIG. 3. In 3T pixel designs, such as that disclosed by Dierickx, however, there is no transfer transistor to segregate the photodiode from a floating diffusion node. Rather, charge generated by the photodiode is accumulated in a charge storage node directly adjacent to the photodiode. See, for example, charge storage node 37 of Dierickx's FIG. 3, which is directly adjacent to photodiode 32. Charge is then readout directly from this charge storage node rather than from a separate floating diffusion region.

Because 3T pixel circuits do not have a floating diffusion region segregated from the photodiode by a transfer transistor, there is no floating diffusion region to be reset by pulsing the reset transistor just prior to the end of the integration period. See, for example, Dierickx's FIG. 5, which illustrates the charge storage node ("signal on node") being reset only *after* the "readout moment." Thus, the operation of the reset transistor taught by Dierickx is incompatible with 4T and 5T pixel designs and would yield images with excessive noise.

For at least all of these reasons, Applicants respectfully submit that substantially adapting the Dierickx disclosure to yield the invention claimed by Applicants would not have been obvious to one of ordinary skill in the art at the time the invention was made. Therefore, the rejection of claim 1 over the Guidash and Dierickx combination should be withdrawn and the claim allowed.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Guidash in view of Dierickx in further view of Ueno (U.S. Patent No. 6,342,920) ("Ueno"). The rejection is respectfully traversed.

The Office Action correctly concludes that the Guidash and Dierickx combination does not teach or suggest the particular signal characteristics recited in claims 6 and 7. Therefore, the Office Action relies on Guidash and Dierickx in further combination with Ueno. However, as discussed above, the Guidash and Dierickx combination also fails to teach or suggest other limitations of claim 1, from which claims 6 and 7 depend. Ueno does not cure the failings of the Guidash and Dierickx combination. For at least this reason, the rejection of claims 6 and 7 should be withdrawn and the claims allowed.

Claims 24-30 and 43-53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kochi (U.S. Patent No. 6,974,088) ("Kochi") in view of Dierickx. The rejection is respectfully traversed.

Similar to the rejection of claim 1 over Guidash and Dierickx, the Office Action relies on Kochi as disclosing certain structural elements of the claimed invention when making out the rejection of claim 24, but the Office Action correctly concludes, "Kochi does not disclose applying saturation control signals as claimed." (Page 12) It would not have been obvious to combine Kochi and Dierickx in the manner claimed for substantially the same reason it would not have been obvious to similarly combine Guidash and Dierickx. Dierickx teaches adding another transistor (i.e., a "reference" transistor) to a pixel circuit. By contrast, Applicant claims applying a "saturation control signal" to an existing transistor (e.g., the transfer transistor). This provides efficiency and reduced fabrication costs not realized by the Dierickx design. Therefore, the rejection of claim 24 over the Kochi and Dierickx combination should be withdrawn and the claim allowed.

Claims 25-30 depend from claim 24 and are allowable over the Kochi and Dierickx combination for at least the reasons stated above with respect to claim 24 and on their own merits. Therefore, the rejection of claims 25-30 should be withdrawn and the claims allowed.

Claim 43 recites similar limitations as claim 24 and is allowable over the Kochi and Dierickx combination for at least the reasons stated above with respect to claim 24 and on its own merits. Therefore, the rejection of claim 43 should be withdrawn and the claim allowed.

Claims 44-53 depend from claim 43 and are allowable over the Kochi and Dierickx combination for that least the reasons stated above with respect to claim 43 and on their own merits. Therefore, the rejection of claims 44-53 should be withdrawn and the claims allowed.

Claims 19-23 and 37-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al. (U.S. Patent No. 7,002,626) ("Pain") in view of Dierickx. The rejection is respectfully traversed.

Similar to the rejection of claim 1 over Guidash and Dierickx, the Office Action relies on Pain as disclosing certain structural elements of the claimed invention when making out the rejection of claim 19, but the Office Action correctly concludes, "Pain does not disclose applying saturation control signals as claimed." (Page 17) It would not have been obvious to combine Pain and Dierickx in the manner claimed for substantially the same reason it would not have been obvious to similarly combine Guidash and Dierickx or Kochi and Dierickx. Dierickx teaches adding another transistor (i.e., a "reference" transistor) to a pixel circuit. By contrast, Applicant claims applying a "saturation control signal" to an existing transistor (e.g., the transfer transistor). This provides efficiency and reduced fabrication costs not realized by the Dierickx design. Therefore, the rejection of claim 24 over the Pain and Dierickx combination should be withdrawn and the claim allowed.

Claims 20-23 depend from claim 19 and are allowable over the Pain and Dierickx combination for the at least the reasons stated above with respect to claim 19 and on their own merits. Therefore, the rejection of claims 20-23 should be withdrawn and the claims allowed.

Claim 37 recites similar limitations as claim 19 and is allowable over the Pain and Dierickx combination for at least the reasons stated above with respect to claim 19 and on its own merits. Therefore, the rejection of claim 37 should be withdrawn and the claim allowed.

Claims 38-42 depend from claim 37 and are allowable over the Pain and Dierickx combination for at least the reasons stated above with respect to claim 37 and on their own merits. Therefore, the rejection of claims 38-42 should be withdrawn and the claims allowed.

New claim 54 recites limitations similar to claim 1 but further recites the times at which the transfer and reset transistors are partially or fully turned on. Claim 54 is allowable over the cited art for at least the reasons stated above with respect to claim 1 and on its own merits.

In view of the above, Applicants believe the pending application is in condition for allowance and respectfully request that it be passed to issue.

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Respectfully submitted,

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